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A double-sampling cross noise-coupled split $\Sigma\Delta$-modulation A/D converter with 80 dB SNR.

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***Abstract*—This paper presents the design of a double-sampling split $\Sigma\Delta$-modulation analog-to-digital converter with cross noise-coupling. Double-sampling is used to achieve high conversion speed and low power consumption. To tackle the problem of quantization noise folding due to path mismatch, a fully floating bilinear integrator is used. Then the quantization noise is cross-coupled between two identical $\Sigma\Delta$-modulators. This increases the effective noise shaping order of this structure with one. The final design is an optimized second order double-sampling split $\Sigma\Delta$-modulator with third order noise shaping through cross noise-coupling. This design is simulated at transistor level in an 0.18-μm CMOS process for 80 dB SNR and 5 MHz bandwidth.**

***Index Terms*—Analog-to-digital converters, double sampling, $\Sigma\Delta$-modulation, noise-coupling, 0.18 μm CMOS technology**

I. Introduction

Modern wireless communication systems such as WLAN or UMTS require high-speed and high-resolution analog-to-digital (A/D) converters. Sigma-Delta ($\Sigma\Delta$)-modulation is a proven technique to realize the desired resolution. To attain the high accuracy oversampling and noise shaping are used. A discrete time $\Sigma\Delta$-modulator is implemented with switched capacitor (SC) circuits. The efficiency of SC-circuits can be easily doubled by using double-sampling techniques. In double-sampling SC-circuits, the outputs are updated during both clock phases of the master clock. This way, the sampling frequency is twice the master clock frequency and for the same power budget the oversampling ratio (OSR) is doubled. Unfortunately, conventional double-sampling $\Sigma\Delta$-modulators are sensitive to path mismatch, which causes quantization noise to fold back into the signal band. Therefore a fully floating bilinear input branch will be used. Such a circuit does not suffer from noise folding. However, for the use of a bilinear input branch the structure of the modulator loop must be slightly adapted [1].

In split architecture $\Sigma\Delta$-modulators, two identical modulator loops are used in parallel. For such architectures, cross noise-coupling can be used [2], [3]. The quantization noise of one modulator loop is injected at the quantizer input of the other modulator loop and vice versa. Due to thermal noise domination, there will be no correlation between the quantization noises of both modulator loops. Therefore the injected quantization noise will act as a dither signal and will not change the normal operation of a single modulator loop. In [4] it is shown that cross noise-coupling can lead to significant reduction in power consumption when applied to low order modulators.

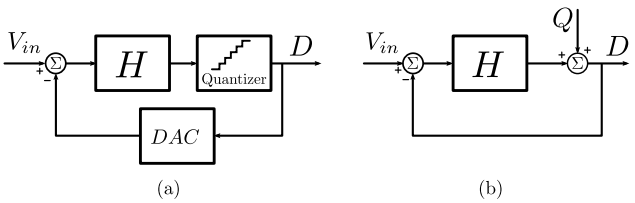

Fig. 1. (a) The $\Sigma\Delta$-modulator and (b) the linearized model.

In this paper, we combine double-sampling with cross noise-coupling. Section II highlights the design issues regarding double-sampling $\Sigma\Delta$-modulation and the use of a bilinear integrator. In section III the technique of cross noise-coupling is discussed. Then in section IV, these two techniques are combined for an optimal system-level design. In section V the analog design considerations are highlighted. Section VI shows the simulation results for the $\Sigma\Delta$-modulator at transistor level. Finally, in section VII a conclusion is presented.

II. Double-Sampling

Fig. 1(a) shows the conceptual diagram of a $\Sigma\Delta$-modulator. The quantizer is embedded in a control loop with loop filter H. The digital output D of the quantizer is fed back to the input of the filter via a digital-to-analog converter (DAC). A common analysis for this system is shown in fig. 1(b). Here, the quantizer is modeled as an additive white noise contribution Q and the D/A-converter for the feedback path is assumed to be ideal. The digital output D of the complete system can then be written as:

$$D(z) = \underbrace{\frac{H(z)}{1+H(z)}}_{\text{STF}(z)} V_{in} + \underbrace{\frac{1}{1+H(z)}}_{\text{NTF}(z)} Q(z) \qquad (1)$$

Here, STF(z) corresponds to the signal transfer function and NTF(z) to the noise transfer function. The main building block in the loop filter H is an integrator. The magnitude of the loop filter will be high in the low-pass signal band, but very low outside the signal band. This way the NTF will be nearly zero in the signal band but not outside the signal band. The quantization noise is thus shaped outside the signal band and

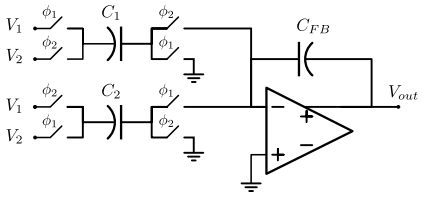

Fig. 2. A conventional double-sampling integrator circuit.

the output has a very high signal-to-noise-plus-distortion ratio (SNDR) within the signal band. As the STF will be close to unity in the signal band, we can approximate (1) to:

$$D(z) \approx V_{in}(z) + \text{NTF}(z)Q(z) \tag{2}$$

A conventional double-sampling SC integrator circuit is shown in fig. 2. It consists of an operational amplifier with a fixed feedback capacitor C_{FB} and two input branches with matched capacitors C_1 and C_2. For the two input branches the switches operate alternatively which make them work in tandem. The output of this circuit can be written as:

$$V_{out} = \frac{C_1}{C_{FB}} \frac{(z^{-1}V_1 - V_2)}{(1 - z^{-1})} \tag{3}$$

However, C_1 and C_2 can never be perfectly matched. We denominate this mismatch $\delta = (C_1 - C_2)/(C_1 + C_2)$. Due to this mismatch, a conventional double-sampling integrator will fold signals around half the sampling frequency ($f_S/2$) to the baseband [1]. The performance of the $\Sigma\Delta$-modulator is then degraded, as the shaped quantization noise is folded back into the signal band. We will call this additional noise contribution N_{fold} and the output of the modulator can now be written as:

$$D(z) \approx V_{in}(z) + \text{NTF}(z)Q(z) + N_{fold}(z) \tag{4}$$

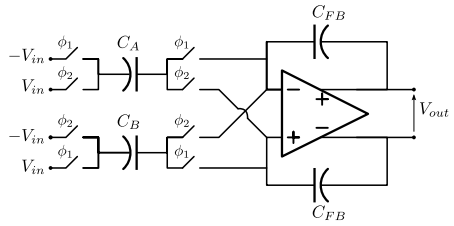

Fig. 3. Fully-floating bilinear integrator circuit.

If $V_2 = -V_1$ for the circuit in fig. 2, we obtain a bilinear double-sampled integrator:

$$V_{out}(z) = \frac{C_A}{C_{FB}} \frac{(1 + z^{-1})}{(1 - z^{-1})} V_1(z) \tag{5}$$

Fig. 3 shows an alternative implementation of a bilinear double-sampled integrator [1], [5]. The input branch is a fully-floating cross-coupled double-sampled input circuit with two matched capacitors C_A and C_B. It can be shown that for this circuit, mismatch between C_A and C_B does not lead to signal folding [5].

Fig. 4 shows one of the modulator architectures proposed in [1]. All the n integrators have a conventional delaying input

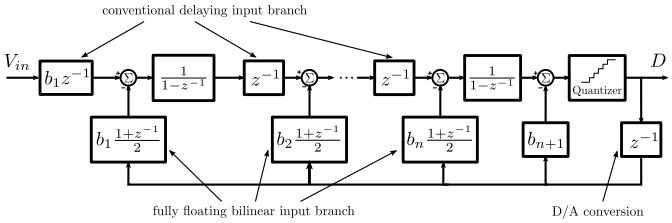

Fig. 4. A modulator architecture suitable for double-sampling.

branch connected to the previous stage, but the feedback path for the output D is implemented with the fully-floating bilinear input branch. The extra delay in the feedback path is due to the combination of the quantizer and the D/A converter. Since the bilinear transfer function introduces an extra delay in the feedback path, the order of the loop filter will be $n + 1$. But as there are only n integrators, there are only n NTF zeros in the low-pass baseband and thus:

$$\text{NTF}(z) = \frac{z(z-1)^n}{P_{n+1}(z)} \tag{6}$$

To have total controllability on the placement of the NTF poles, the coefficient b_{n+1} is added. This gives $n + 1$ independent degrees of freedom to place the $n + 1$ poles. In [1] it is shown that the dominant noise folding term now exhibits a second order differentiation:

$$N_{fold}(z) \approx \delta \text{NTF}(-z)Q(-z) \frac{(1 - z^{-1})^2}{2z^{-1}(1 + z^{-1})} \tag{7}$$

The use of a bilinear integrator also has a second advantage as it halves the input capacitance for the integrators. As a result, the operational amplifiers can be designed with less unity gain bandwidth and thus consume less power.

An easy design approach for the NTF of the modulator in fig. 4 is to set one of the poles equal to $z = 0$. Then the other poles are placed in a n^{th} order Butterworth configuration according to [6], [7]. Fig. 5 shows the maximum SNDR achievable for a second and a third order modulator in function of $||H||_\infty$ with a 3 bit quantizer and OSR=16. For these modulators, the baseband zeros are also optimized through local feedback [6]. The mismatch in the conventional double-sampling input branches is $\delta = 0.01$.

III. Noise-coupling

In a split architecture $\Sigma\Delta$ A/D converter, a single modulator is split into two identical halves. As the two resulting modulator loops have capacitors half the size of those in the original modulator, total power dissipation and chip area will remain essentially the same. Each modulator loop processes the same input signal independently of the other loop. The two outputs are then combined to generate the total average output signal D_{av}. Since thermal as well as quantization noise are uncorrelated between the two loops, the SNR performance of the split modulator is the same as for the original single modulator.

The noise added by the quantizer can be determined by taking the difference between the output and the input of

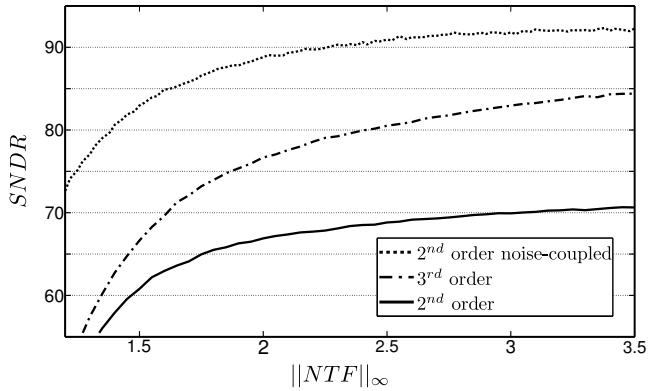

Fig. 5. The SNDR in function of $||NTF||_\infty$ for different modulator structures with OSR=16 and a 3 bit quantizer.

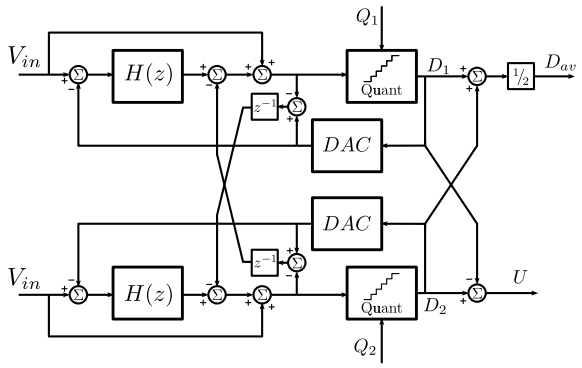

Fig. 6. A split $\Sigma\Delta$-modulator with cross-coupled noise injection.

the quantizer. In [2]- [3] noise-coupled split $\Sigma\Delta$-modulator architectures are presented. In this architecture, the noise of one loop is injected into the other loop as shown in fig. 6. Applying a linear model to both quantizers, the outputs from the loops can be obtained:

$$D_1(z) = V_{in} + NTF_1(z)(Q_1 - z^{-1}Q_2) \tag{8}$$

$$D_2(z) = V_{in} + NTF_2(z)(Q_2 - z^{-1}Q_1) \tag{9}$$

Assuming the NTF's of both modulators are equal, the output signal of the whole structure can be written as:

$$D_{av}(z) = \frac{D_1 + D_2}{2} \tag{10}$$

$$= V_{in}(z) + (1 - z^{-1})NTF(z)\frac{Q_1(z) + Q_2(z)}{2} \tag{11}$$

The noise shaping now exhibits an additional differentiation $(1-z^{-1})$. Hence the effective noise shaping is of order $n+1$. In addition, this noise-coupling does influence the stability of the single modulator loop. The injected quantization noise is uncorrelated with the signals in the receiving loop, and acts as a dither signal. Dithering will reduce the harmonic distortion and as such improves the dynamic range. The only disadvantage is that the peak SNDR will be at a slightly lower input amplitude (relative to full-scale). This can be understood by noting that the power at the quantizer input is increased. Hence, the quantizer itself will be faster overloaded. Fig. 5 shows the peak-SNDR in function of $||NTF||_\infty$ when cross noise-coupling is added to a 2nd order modulator of the architecture shown in fig. 4. For these simulations the OSR $= 16$, $\delta = 0.01$ and the quantizer has 3 bit resolution.

IV. Combined Design

The goal of this design is a low-power low-distortion $\Sigma\Delta$-modulator A/D converter which can achieve 80 dB SNR for a bandwidth of 5 MHz after implementation in a 0.18µm CMOS process. The results shown in fig. 5 show that when cross noise-coupling is added to a second order modulator of fig. 4, a SNDR of 90 dB can easily be achieved. For poles in a second order Butterworth configuration with $||NTF||_\infty = 2$ and the third pole at zero, the modulator coefficients can be rounded to:

$$b_1 = \frac{1}{2}, b_2 = \frac{3}{2}, b_3 = \frac{1}{2} \tag{12}$$

The resulting modulator poles are:

$$z_{1,2} = \frac{3}{8} \pm j\frac{\sqrt{7}}{8} \tag{13}$$

The local feedback coefficient g is then optimized for maximal SNDR performance for D_{av} which gives $g = \frac{1}{64}$.

[8] highlights the importance of having small signal swings at the modulators internal nodes. To achieve this, feed-forward branches for the input signal are provided toward the input of every integrator and the quantizer. Ideally, the loop filter then only has to process quantization noise. As a result, the integrator output then becomes uncorrelated to the input signal. This will make the modulator less susceptible to non-idealities in the loop filter leading to less distortion for the overall modulator. Also, this will reduce the maximum output of the integrators. However, because bilinear branches for the feedback of the modulator output are used, the $STF(z) = 1$ can only be approximately achieved.

The final modulator architecture is shown in fig. 7. The feedback branches for the output signal are implemented with a fully-floating bilinear integrator, while the input signal V_{in} is sampled with a conventional bilinear input branch (fig. 2). This design is simulated at the behavioral level for a capacitance mismatch $\delta = 0.01$ and a quantizer with 9 quantization levels. The peak-SNDR for this design then becomes 91 dB and is attained for an input amplitude of -1.9 dB. The maximum output of the first integrator stays within 50 % of the signal full-scale. For the second integrator this becomes 70 %.

V. Analog implementation

The modulator is designed in a 0.18 µm CMOS process with a supply voltage of 1.8 V. The implementation of the modulator is fully differential and the signal bandwidth is chosen to be 5 MHz. At the intended oversampling ratio of 16, this corresponds to a sampling frequency of 160 MHz. However, because of the double-sampling, the master clock frequency is only 80 MHz.

The quantizer has 9 quantization levels for a differential full-scale of ± 1 V. The feedback branches then consist of 4

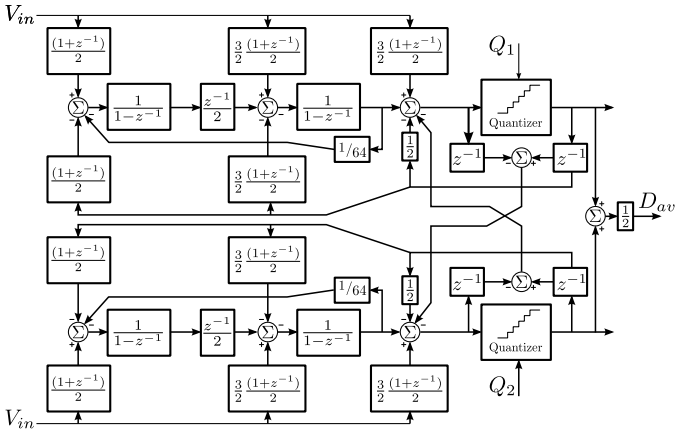

Fig. 7. The implemented modulator architecture.

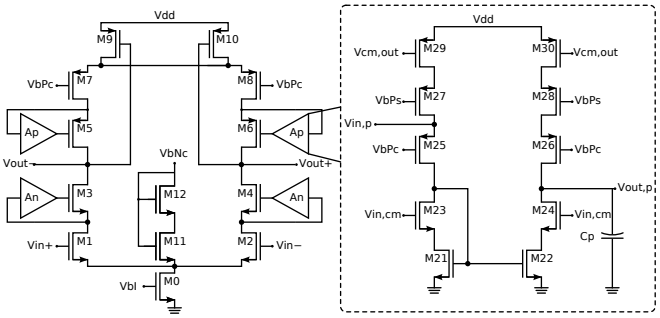

Fig. 8. The circuit for the operational amplifier used in the integrators.

identical capacitors which input can be switched to $+V_{ref}$, V_{cm} or $-V_{ref}$. Due to kT/C-noise in SC-circuits, the overall SNR performance of the implementation will be controlled by the capacitance of the capacitors. Since the peak-SNDR is attained for a -2 dB input tone, the capacitances are chosen such that the noise floor is at maximum 85 dB to achieve the desired 13-bit accuracy. For the implementation of the switches a standard CMOS-switch is used.

The op-amp used for the integrators is shown in fig. 8. Because of the low output swing of the integrators, a telescopic cascode op-amp is chosen (see section IV). System level simulations showed a DC-gain of at least 55 dB was necessary. To achieve this high gain the cascode transistors are boosted with a high-swing low-voltage regulation amplifier [9]. The booster for the PMOS cascode is also shown in fig. 8. To attain an accurate settling behavior, the boosters are band limited by adding small capacitors in their outputs. The common-mode output is regulated by triode transistors M9-M10 which act as an adjustable current source. For the adder, a folded cascode op-amp is used to attain the differential full-scale of ± 1 V at the input of the quantizer. For this op-amp gain boosting and common mode feedback are made in a similar way.

VI. Simulation results

The entire modulator is simulated at transistor level with a -2 dB input tone with frequency 1.6 MHz. The master clock frequency is 80 MHz. The SNDR for the output of a single loop is 56 dB. Fig. 9 shows the fast Fourier transform of the combined output of the split $\Sigma\Delta$-modulator. The extra zero due to cross noise-coupling is noticeable at DC. The SNDR for the total output is 91.2 dB. This gives the amplifier headroom for sizing the circuit in a noise limited way. The analog part of the circuit consumes a total of 11 mW.

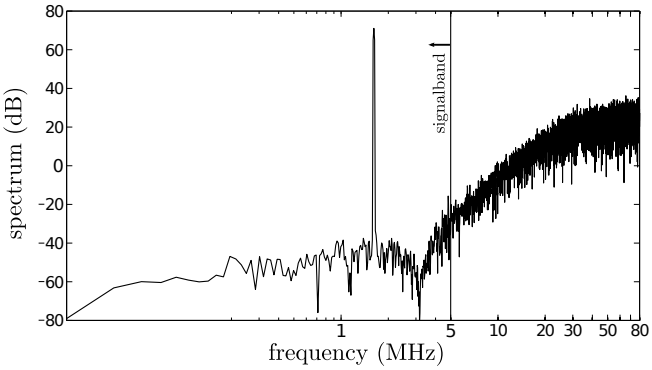

Fig. 9. FFT of the output signal.

VII. Conclusion

A 5 MHz bandwidth $\Sigma\Delta$-A/D converter with 13-bit accuracy is presented. The design consists of a split 2nd order double-sampling modulator with cross noise-coupling. To tackle the problem of quantization noise folding in a double-sampling SC-circuit, a fully floating bilinear input branch is used for the feedback of the D/A-converter. By adding cross noise-coupling between the two identical loops of the split modulator, the effective noise shaping order is increased to 3. The modulator is then optimized for an oversampling ratio of 16 and a 3-bit quantizer. The final design is implemented in an 0.18-µm CMOS process. The analog implementation is then validated through simulation. The analog circuits consume a total of 11 mW.

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